ERROR DETECTING CIRCUIT
FOR DETECTING THE LOCATION OF ERROR

Abstract of the Disclosure

An error detecting circuit for quickly detecting the location of an error is provided. The error detecting circuit has an error data storing unit and an error data collecting unit. The error data storing unit divides a circuit which is implemented in a chip into predetermined areas and outputs a plurality of error signals in response to a plurality of state error signals, a serial chain signal, a lock-enable signal, and a chip error signal. Each of the plurality of state error signals is enabled when an error occurs in the corresponding predetermined area. The serial chain signal is for reading the plurality of state error signals stored in the chip if the chip goes out of order when an error occurs in the circuit implemented in the chip. The lock-enable signal is for determining whether or not to preserve the plurality of the generated state error signals. The error data collecting unit outputs the chip error signal in response to the plurality of error signals output from the error data storing unit. The error data storing unit stores and outputs at least one of the plurality of state error signals and, in response to the serial chain signal, enables a confirmation of at least one of the state error signals stored in the error data storing unit.